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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,516	02/21/2002	Antonin Rozsypal	ONS00301	4702

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EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 07/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,516	ROZSYPAL, ANTONIN	
	Examiner	Art Unit	
	Blane J Jackson	2685	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-17* is/are allowed.

6)☒ Claim(s) *1,9,10,13 and 18* is/are rejected.

7)☒ Claim(s) *2-8,11,12, 17,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities: Claim 17 states dependency on claim 11 where a dependency on claim 13 is expected. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wan et al. (U.S. Patent 6,265,939) with a view to Abe et al. (U.S. Patent 6,710,716).

As to claim 1, Wan teaches an integrated detector circuit comprising:

A first *diode detector stage* having an input that monitors a high frequency signal for routing a first detection current to a node (figure 2, diode stage D1, coupled sample of the RF output of the PA is the high frequency signal and node is the differential line B,),

A second *diode detector stage* including a first current source for supplying a bias current indicative of a predefined amplitude of the high frequency signal (figure 2, diode stage D3 (or D4), coupled sample of the RF output of the PA is the high

frequency signal) and having an input for monitoring the high frequency signal to route a portion of the bias current to the node as a second detection current wherein the second detection current is limited to the bias current when the high frequency signal is greater than the predefined amplitude (RF sampled input and biasing of diodes: column 2, lines 32-55, operation is sequential conduction of three diode stages D1 to D3 to D4 to maintain a linear bias current or voltage summed at node G: column 3, lines 8-53. Wan shows detector circuit gain is provided in a differential op amp in figure 2).

Wan teaches a plurality of diode detector stages followed by a bias gain element but does not teach a first and second gain stage.

Abe teaches an RF power detecting circuit suited for monolithic structures with linearity of the detection characteristic operating at a frequency greater than 1.5 GHz (figures 7-12, column 9, lines 29-37). Abe teaches a gain stage comprising FETs or other active elements with bias control configured with a single or differential input but a differential output to control any DC offset (figures 7-12, column 11, lines 3-22). Abe teaches the advantages of the active element over several conventional prior art type detector stage using a single diode peak detector or a Si MOSFET and their associated poor linear performance (figures 1-4, column 1, line 19 to column 2, line 37).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the sequential bias current diode based contribution stages of Wan with the active gain stages of Abe such that the circuit maintains a differential output and better suited for high frequency broadband applications and monolithic structures.

As to claims 10 and 18, Wan teaches a detector circuit comprising *diode detector stages* that include current sources (diode stages and biasing D1, D3 and D4 of figure 2) for establishing maximum current levels in the gain stages at corresponding amplitudes of a high frequency signal wherein the gain stages function with transfer functions that convert the high frequency signal to detection currents for summing at a common node (node G) to produce an output detection signal as a substantially linear function of the high frequency signal (figure 1) wherein the detection currents reach the maximum current levels at the corresponding amplitudes to compensate for nonlinearities in the transfer functions (RF sampled input and biasing of diodes: column 2, lines 32-55, operation is sequential conduction of three diode stages D1 to D3 to D4 to maintain a linear bias current or voltage summed at node G: column 3, lines 8-53).

Wan teaches a plurality of diode detector stages followed by a bias gain element but does not teach gain stages.

Abe teaches an RF power detecting circuit suited for monolithic structures with linearity of the detection characteristic operating at a frequency greater than 1.5 GHz (figures 7-12, column 9, lines 29-37). Abe teaches a gain stage comprising FETs or other active elements with bias control configured with a single or differential input but a differential output to control any DC offset (figures 7-12, column 11, lines 3-22). Abe teaches the advantages of the active element over several conventional prior art type detector stage using a single diode peak detector or a Si MOSFET and their associated poor linear performance (figures 1-4, column 1, line 19 to column 2, line 37).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the sequential bias current diode based contribution stages of Wan with the active gain stages of Abe such that the circuit maintains a differential output and better suited for high frequency broadband applications and monolithic structures.

Allowable Subject Matter

3. Claims 13-16 are allowed. The prior art made of record fails to teach a method of detecting a high frequency signal comprising the step of limiting the first detection current to a constant value to compensate for a nonlinearity in the second transconductance where the high frequency signal is greater than a predefined amplitude.

4. Claims 2-8, 11, 12, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nicholas et al. (U.S. Patent 4,502,015) disclose a bridge diode detector followed by an amplifier with feedback to enhance linearity on operation. Klotz (U.S. Patent 4,816,772) discloses an AGC amplifier with a linearization circuit to provide a linear gain response over a wide dynamic range. Benton et al. (U.S. Patent

5,079,454) discloses a RF detector comprising FET gain stages configured for differential output and temperature compensation. Aihara (U.S. Patent 5,214,393) discloses a conventional RF power control circuit with a diode detecting circuit, amplifier and comparison error amplifier in the feedback path. De Loe, Jr. (U.S. Patent 5,603,113) discloses a automatic gain control circuit for both receiver and transmitter adjustable amplifier including a linear signal level detector. Jensen et al. (U.S. Patent 5,724,003) discloses a method for power control with user supplied adjusted gain in the feedback path such that the operation of the rectifying power detector is maintained in a linear region. Brown et al. (U.S. Patent 6,259,682) discloses power control for a transmitter having means for maintaining constant loop gain for stability and accuracy over a wide range of RF power levels. Fujita et al. (U.S. Patent 5,329,244) discloses a conventional feedback circuits using diode power detectors to control the amplitude and phase for linear compensation to a high frequency power amplifier. Shoulders et al. (U.S. Patent 6,212,479) discloses a super heterodyned power detector with enhance linearity for use in power leveling loops.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J Jackson whose telephone number is (703) 305-5291. The examiner can normally be reached on Monday through Friday, 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (703) 305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BJJ

Quochien B. Vuong 7/12/04

QUOCHIEN B. VUONG
PRIMARY EXAMINER